REMARKS

Claims 25-47 are rejected. Claims 25-47 are pending. Claims 25, 29-32, 36, 37 and 39-47 are amended.

Claims 25-47 are rejected under 35 USC 102(e) as being unpatentable over Shipton (US 2006/0052962). The examiner relies on Shipton as a 102(e) reference to anticipate the features of the present claim. Respectfully, the present application claims priority to German Patent Application No. 10 2004 008809.8, which was filed on February 20, 2004. Thus, the 102(e) date of the present application is February 20, 2004. Shipton, however, was filed on August 29, 2005, over 18 months after the priority date of the present application. Thus, Shipton is not a proper 102(e) references, and rejection under 102(e) over Shipton is improper.

Even if Shipton were a proper 102(e) reference, Shipton fails to disclose all the features claimed in each of the independent claims 25, 39 and 41. In the examiner's remarks, the examiner responds to the applicant's previous arguments that the reference does not teach an error checking circuit with multiple independent processor cores, as is claimed in the "respective first and second independent processor cores" feature of claim 25 by citing LSS Bus 0 master unit and LSS Bus 1 master unit of Figure 80 of Shipton as disclosing multiple processor cores. The claimed feature requires the use of either a single processor with multiple independent cores or multiple independent processors. Contrary to this, Figure 80 of the cited reference discloses only a single processor (CPU). Nothing in the disclosure of Shipton describes or implies that the CPU includes multiple processors cores, nor is such a feature inherent in processors.

Respectfully, the examiner's interpretation of the LSS Master Units of paragraphs 1666 and 1668 as well as Figure 80, as being processor cores is inconsistent with both the standard use of the term "processor core" and the specification of Shipton. The specification of Shipton explicitly describes a single processor core as part of the CPU. Furthermore, the LSS master Units cannot be interpreted as processor cores because they aren't components of the processor.

As explained at paragraph 488 of Shipton, Shipton uses the term CPU to define a "CPU core, caching system, and MMU." Thus, Shipton clearly defines the CPU of Figure 80 as containing a processor core. As Shipton defines the CPU as including the processor core,

interpreting the LSS bus master units as processor cores is inconsistent with the specification of Shipton, and is improper.

As the examiner's 102(e) rejection relies on an improper interpretation of Shipton, and, when properly interpreted, Shipton only discloses a single processor core, Shipton cannot anticipate claims 25-47, and the rejection is improper.

Applicant believes that no additional fees are necessary, however, the Commissioner is authorized to charge Deposit Account No. 50-1482 in the name of Carlson, Gaskey & Olds, PC for any additional fees or credit the account for any overpayment.

Respectfully submitted,

/Stephen A. Burch/
Stephen A. Burch, Reg. No. 66,570
Carlson, Gaskey & Olds
400 W. Maple Road, Ste. 350
Birmingham, MI 48009
(248) 988-8360

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